Multiphase Current Controlled Buck Converter with Energy Recycling Output Impedance Correction Circuit (OICC): Adaptive Voltage Positioning (AVP) and Dynamic Voltage Scaling (DVS) application

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Abstract— **Modern microprocessors impose strict specifications on Voltage Regulating Modules (VRMs) with advanced features such as Dynamic Voltage Scaling (DVS) and Adaptive Voltage Positioning (AVP). In this study the Output Impedance Correction Circuit (OICC) concept is employed as an additional energy path in a Multiphase synchronous buck converter in a manner that, during the load steps transients, the output capacitor of 150 µF is virtually increased to 2.1 mF, thus improving the response under AVP operation. On the other hand, during the output voltage reference step, the OICC is inactive, facilitating DVS operation and reducing the current stress on the switches and the inductors. Furthermore, the proposed solution is compared with a reference converter with 2.1 mF output capacitor, for both AVP and DVS operations. The OICC is implemented as a Synchronous Buck Converter with Peak Current Mode Control (PCMC), having smaller penalty on the system efficiency comparing with Linear Regulator (LR) implementation.**

Keywords—component; formatting; style; styling; insert (key words)

I. INTRODUCTION

In Voltage Regulation Module (VRM) applications, it is well known that the main driver in designing the output filter stage is the output impedance of the system due to the strict specifications imposed by the load [1], [2]. In addition, advance features, such as Dynamic Voltage Scaling (DVS) and Adaptive Voltage Positioning (AVP), impose opposite trends on the output capacitor design: for load steps, big capacitor is favorable, while for the output voltage reference step, smaller capacitor is favorable. Therefore, the ongoing research trend is directed to improve the dynamic response of the VRM while reducing the size of the output capacitor by means of either improving the controller [3]-[8], or by introducing an additional energy path to compensate the charge perturbation of the output capacitor [9]-[22].

The dynamic behavior of the system with a linear control (Voltage mode control, VMC, Peak Current Mode Control, PCMC,...) is limited by the converter switching frequency. The reduction of the output capacitor can be achieved by increasing the switching frequency of the converter, thus increasing the bandwidth of the system. The drawback of this approach is that the system efficiency is penalized due to increased switching losses and RMS currents. In order to achieve both the output capacitor reduction and high system efficiency, while satisfying strict dynamic specifications, a Multiphase converter system is adopted as a standard for VRM applications [3]. In order to ensure the current sharing among the phases, the multiphase converter is usually implemented with current mode control.

The second possibility to reduce the output capacitor is to introduce an additional energy path to compensate the charge unbalance of the output capacitor [9]-[22], consequently reducing the transient time and output voltage deviation. Doing so, during the steady-state operation the system has high efficiency because the main low-bandwidth converter is designed to operate at moderate switching frequency, whereas the dynamic behavior is determined by the high-bandwidth auxiliary energy path, during the load-step transients. The auxiliary energy path can be implemented as a resistive path ([9], [10]), as a Linear regulator, LR, ([11]-[13], [19], [20]), or as a switching converter ([14]-[18], [21], [22]). The first two implementations provide faster response, at the expense of increasing losses during the transient. On the other hand, the switching converter implementation presents lower bandwidth, limited by the auxiliary converter switching frequency, though it produces smaller losses compared to the two previous implementations.

The Output Impedance Correction Circuit (OICC) concept, employed in this study, has been presented in [19] and analyzed in detail in [20], while the concept is extended to multiphase solutions in [21] and analyzed in detail in [22]. This solution utilizes an additional energy path, provided by the OICC, so that the auxiliary current, injected/extracted through this path is controlled to have n-1 times higher value than the output capacitor current with appropriate directions. Doing so, the OICC creates an equivalent n times bigger virtual capacitor at the output, thus reducing the output impedance for AVP operation. On the other hand, for DVS operation, the OICC remains inactive, thus the output voltage step is performed with smaller, nominal capacitor. In order to measure the output

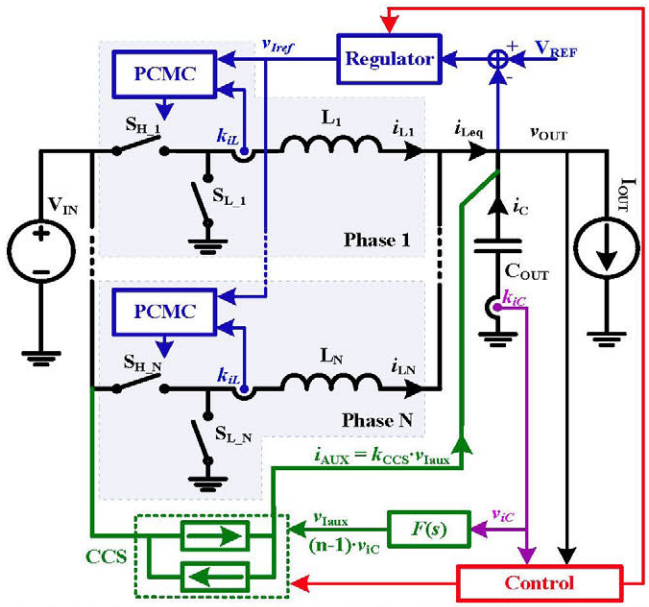

Fig. 1. Multiphase Buck Converter with the OICC – Multiphase Buck converter (black), the current measurement, driving signal generation and the regulator (blue), non-invasive current sensor (purple), the OICC (green) and system control (red).

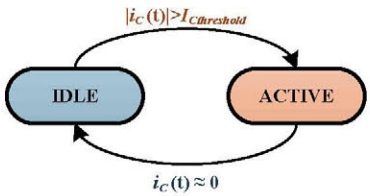

Fig. 2. The State machine of the control system).

capacitor current, a noninvasive current estimator from [23] is used. The proposed solution has been designed with a physical output capacitor of 140 µF and a virtual capacitor of 2.1 mF. Furthermore, the solution has been compared with a reference design, which has the same power stage with the difference that the physical output capacitor is 2.1 mF. Both prototypes are compared under APV and DVS operation, showing that the OICC solution has the same behavior as the reference design under AVP operation, while improving DVS operation.

II. The Output Impedance Correction Circuit – Basic Operation

A Multiphase buck converter with Peak Current Mode Control (PCMC) and with the OICC is shown in Fig. 1. The system utilizes the OICC in a manner that the OICC injects/extracts a current in the output node that is n-1 times bigger than the output capacitor current with their corresponding directions. This behavior of the OICC virtually increases the output capacitance n times during the load-steps transients, thus reducing the output impedance by the same factor. The system is composed of the Multiphase Buck converter (black) with a slow regulator (blue), which can be dynamically modified, the OICC (green - power stage, purple - current measurement) behaving like a controlled current source CCS and the system control (red). The control block allows the OICC to inject/extract the current only in certain states of the transient routine. At the same time, in order to maintain the stability of the system, the control modifies the main converter regulator.

During the steady-state, the OICC is inactive; all the energy is transferred through the Multiphase buck converter and it is behaving like a voltage source, while the system control is sensing the output capacitor current in order to initialize the transient routine when a load step occurs. In this manner, by sensing the output capacitor current, the system reacts nearly instantaneously to any load perturbation, since the output capacitor current is the fastest variable in the system that detects this perturbation. When the load step occurs, the OICC is activated and the output impedance correction starts. The system controller, implemented as a state machine in Fig. 2, is triggered by the output capacitor current and the system changes to the Active state. In this state, the OICC is providing n-1 times more current than the output capacitor, thus reducing the amount of charge extracted/injected from/to the output capacitor. As a result, the voltage perturbation is smaller. On the other hand, when the output-voltage reference step occurs, the OICC is not activated and the DVS operation is performed with small capacitor.

III. AVP-PCMC Main Buck Converter Regulator Implementation: The OICC Impact

In order to achieve AVP behavior, various strategies can be applied to design the main converter regulator [5]. In CMC controlled converter, the simplest implementation is that the regulator generates the inductor current reference proportionally to the output voltage error, creating specified output voltage drop. Doing so, the error is not canceled, leaving more room for the voltage deviation under the load steps. In the proposed solution, the converter behaves like hybrid system with two different control-to-output transfer functions, v_{OUT}/i^*_{ref}, depending on the state of the system: *Idle* or *Active* state. In order to have desired behavior, the regulator needs to be implemented in that manner to achieve the same load-line resistance R_{LL} in both states. In following analysis this issue is addressed.

A. Stability analysis

The small signal behavior of the system can be modeled for both states as presented in Fig. 3. During the *Idle* state (Fig. 3*a*), the OICC is inactive and the output capacitor is the nominal, thus the transfer function from the inductor current reference, v_{Iref}, to the output voltage, v_{OUT}, is

$$G^{Idle}_{vIref\_vout} = \frac{\hat{v}_{OUT}}{\hat{v}_{Iref}} = \frac{N_{ph}}{k_{iL}} Z_{Cout} = \frac{N_{ph}}{k_{iL}} \frac{1}{sC_{OUT}} \quad (1)$$

where N_{ph} is the number of the phases of the multiphase buck converter, k_{iL} is inductor current gain and Z_{Cout} is the impedance of the output capacitor. On the other hand, during the *Active* state (Fig. 3b), the OICC is active and the OICC subsystem affects the converter transfer function. In order to ensure stability of the OICC subsystem, its open-loop gain needs to be limited and, assuming unity gain of the capacitor current estimator k_{iC} and k_{CCS}, it is

$$L_{OICC} = F(s) = \frac{v_{Iaux}(s)}{v_{iC}(s)} = \frac{n-1}{1 + \frac{s}{2\pi f_{OICCc}}} \quad (2)$$

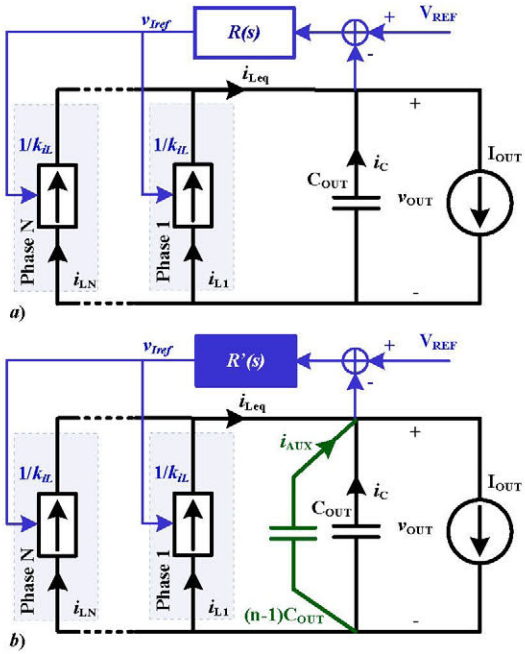

Fig. 3. Averaged models of the system during a) the *Idle* and b) *Active* state.

where n is the multiplication factor and f_{OICCc} is the OICC corner frequency, a frequency up to which the OICC has constant gain n-1. The bandwidth of the OICC subsystem, BW_{OICC}, is (n-1) f_{OICCc}. During the *Active* state, the impedance of the equivalent virtual output capacitor, Z_{Cout}^{EQ}, is defined by

$$Z_{Cout}^{EQ} = \frac{Z_{Cout}}{1+L_{OICC}} = \frac{Z_{Cout}\left(1+\frac{s}{2\pi f_{OICCc}}\right)}{n\left(1+\frac{s}{2\pi n f_{OICCc}}\right)} \tag{3}$$

The OICC reduces the impedance of the output capacitor by factor n in a frequency range below the OICC corner frequency and, since it needs to be bigger than the main converter bandwidth *BW* [22], in the frequency range of interest, the converter model presented in Fig. 3*b*) is valid. The converter transfer function during the *Active* state is

$$G_{vIref\_vout}^{Active} = \frac{\hat{v}_{OUT}}{\hat{v}_{Iref}} = \frac{N_{ph}}{k_{iL}} Z_{Cout}^{EQ} = \frac{N_{ph}}{k_{iL}} \frac{1}{snC_{OUT}} \tag{4}$$

The closed loop output impedance of the system is affected by the open loop gain of the converter during both states defined by

$$\begin{aligned} L_{Idle}(s) &= R(s)G_{vIref\_vout}^{Idle} \\ L_{Active}(s) &= R'(s)G_{vIref\_vout}^{Idle} \end{aligned} \tag{5}$$

where *R(s)* and *R'(s)* are regulators for *Idle* and *Active* state, respectively. Finally, the closed loop output impedance of the system is defined by

$$\begin{aligned} Z_{OUT}^{Idle} &= \frac{Z_{Cout}}{1+R(s)G_{vIref\_vout}^{Idle}} \xrightarrow{f<BW} \frac{k_{iL}}{N_{ph}R(s)} \\ Z_{OUT}^{Active} &= \frac{Z_{Cout}^{EQ}}{1+R'(s)G_{vIref\_vout}^{Active}} \xrightarrow{f<BW} \frac{k_{iL}}{N_{ph}R'(s)} \end{aligned} \tag{6}$$

In order to achieve AVP behavior, as seen in (6), the output impedance depends on the regulator design, so both regulators need to create the same load-line resistance, R_{LL}. Assuming that the open loop output impedance during the *Idle* state has higher value than R_{LL} ($|Z_{Cout}(jw_{BW})|>R_{LL}$), while during the *Active* state has lower value ($\left|Z_{Cout}^{EQ}(jw_{BW})\right|<R_{LL}$), the regulators are defined by

$$R(s) = \frac{k_{iL}}{N_{ph}R_{LL}} \frac{1+s/z}{1+s/p} \quad \text{and} \quad R'(s) = \frac{k_{iL}}{N_{ph}R_{LL}} \tag{7}$$

where z is a zero of the regulator transfer function and p is a pole. Closing the control loop, (7) can be introduced into (6) and desired low frequency output impedance is achieved:

$$\begin{aligned} Z_{OUT}^{Idle} &= \left(\frac{R_{LL}(1+s/p)}{1+s/z}, f<BW\right) \vee \left(1/sC_{OUT}, f>BW\right) \\ Z_{OUT}^{Active} &= \left(R_{LL}, f<BW\right) \vee \left(1/snC_{OUT}, f>BW\right) \end{aligned} \tag{8}$$

The amplitude characteristics of the output capacitor and closed loop output impedance are presented in Fig. 4 (*Idle* state: blue, *Active* state: red), while the output voltage time response of the closed loop system is presented in Fig. 5. It can be seen from Fig. 4*a*) that the closed loop output impedance Z_{OUT}^{Idle} has bigger value at the bandwidth frequency *BW*, causing an undershoot of the output voltage as presented in Fig. 5 (blue). The bandwidth frequency *BW* is limited due to the switching frequency or large signal stability constrains. On the other hand, during the *Active* state (Fig. 4*b*), the output impedance Z_{OUT}^{Active} is defined by a first order transfer function with a dominant pole at the new bandwidth *BW'*. The bandwidth *BW'* is defined by $1/(2\cdot\pi\cdot R_{LL}\cdot n\cdot C_{OUT})$. The time-domain output voltage response has an exponential transition to a new value as shown in Fig. 5 (red). Furthermore, in Fig. 4 normalized amplitude characteristics of both regulators, R(s) and R'(s), are presented. It can be seen that, below the bandwidth frequency, the output impedance is defined by inverse the regulator transfer function, while above the bandwidth, it is defined by the output capacitor impedance: physical capacitor during *Idle* state and virtual capacitor during *Active* state.

For the presented case, the open-loop gain characteristics for both states are presented in Fig. 6. During *Idle* state (blue), the bandwidth of the system is nominal, BW, while the phase margin PM is 80°. Desired phase margin is achieved by positioning the pole and zero, p and z, of the regulator transfer function R(s), having in mind that the zero should be as higher as possible since it becomes pole in closed loop output impedance during the *Idle* state (8) and it affects the time domain response [24].

On the other hand, the open-loop gain, shown in Fig. 6 (red), is defined as a first order system in the frequency range below the OICC corner frequency, f_{OICCc}. Therefore, the bandwidth of the main converter *BW'* is defined by the load-line resistance and the capacitance of the virtual capacitor and it is $1/(2\cdot\pi\cdot R_{LL}\cdot n\cdot C_{OUT})$. Further, since it is a first order system, the phase margin is 90° if the OICC corner frequency is sufficiently high. Fig. 6 shows the impact on the open-loop

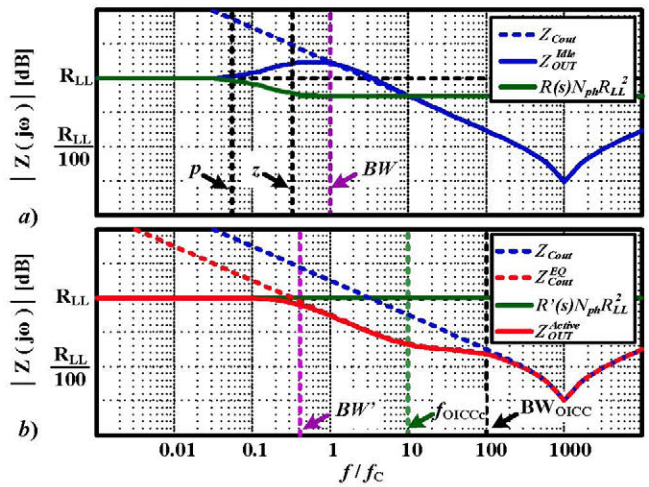

Fig. 4. Amplitude characteristics of the output capacitor impedance (dashed lines) and closed loop (solid lines) impedances of the multiphase converter during: a) *Idle* state (blue lines) and b) *Active* state (red lines); the Regulators R(s) and R'(s) (green lines).

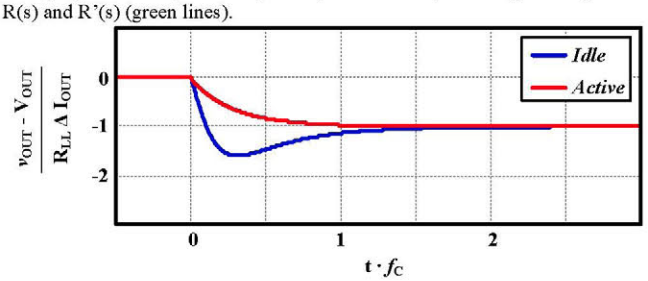

Fig. 5. Normalized load step response of the output voltage of the multiphase converter during *Idle* state (blue line) and *Active* state (red line)

gain of the additional zero and pole of the virtual capacitor defined by (3). Since the zero is at lower frequency than the pole, the phase starts to increase, thus, even if the zero is closer to the bandwidth of the main converter, it would not make the main converter control loop unstable since the phase margin would increase.

B. Main converter Regulator implementation

The AVP operation of the converter system is defined by the regulator implementation, as presented above. Since the converter transfer function is different during *Idle* and *Active* states, in order to maintain the same open-loop characteristic, the regulator needs to be modified as defined by **(7)**. Possible analog implementation is presented in Fig. **7***a*).

The regulator is implemented as inverting amplifier, with an additional analog multiplexer (AMux) and a switch (Sw). Both additional components are controlled by the system controller (red in Fig. 1). During *Idle* state, the control signal *Modify* is low, thus the analog multiplexer is in position 0 and the switch is open. Doing so, series impedance of the resistor R_S and the capacitor C_S is connected in to the feedback branch of the amplifier as presented in Fig. **7***b*). The regulator transfer function is

$$R(s) = \frac{R_1}{R_0}\frac{1+sC_SR_S}{1+sC_S(R_S+R_1)} \tag{9}$$

Comparing both regulator transfer functions given by (7) and (9), regulator components can be calculated from

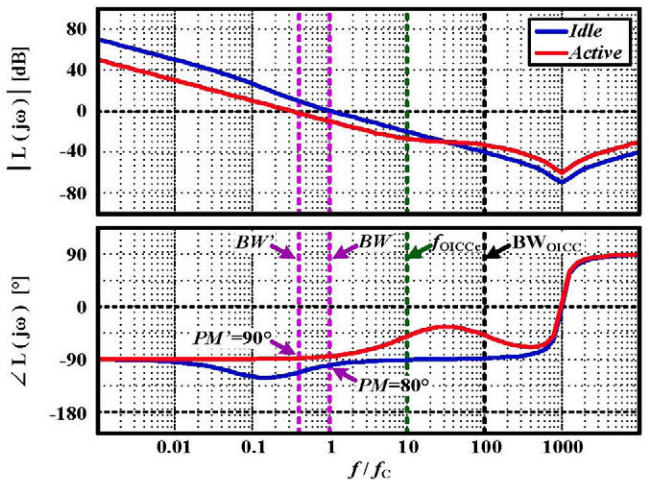

Fig. 6. Amplitude characteristics and Phase characteristic of the open-loop transfer function of the multiphase converter during: a) *Idle* state (blue lines) and b) *Active* state (red lines).

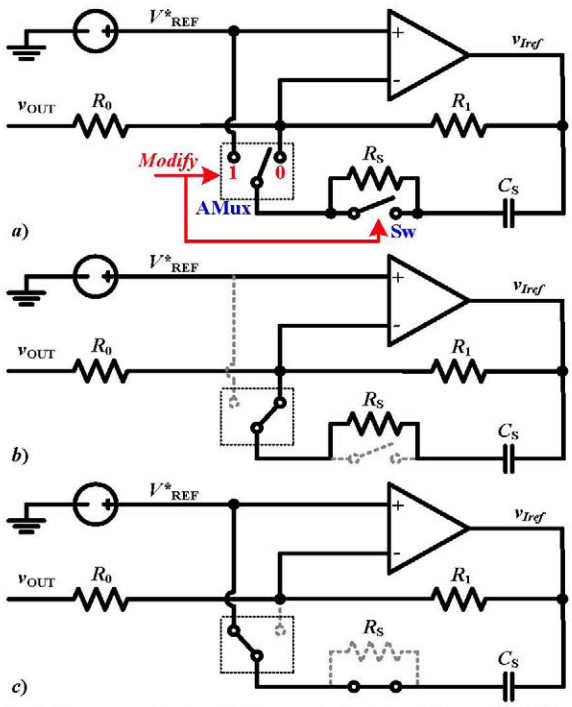

Fig. 7. Main converter regulator – *a*) implementation, *b*) *Idle* state configuration and *c*) *Active* state configuration.

$$\frac{k_{iL}}{N_{ph}R_{LL}} = \frac{R_1}{R_0},\ z = \frac{1}{C_SR_S},\ p = \frac{1}{C_S(R_S+R_1)} \tag{10}$$

On the other hand, during *Active* state, *Modify* signal is high, connecting the analog multiplexer to position 1 and closing the switch, thus configuring the amplifier as presented in Fig. **7***c*). As it can be seen, the feedback branch is composed only of the resistor R_1, defining the regulator transfer function as

$$R'(s) = \frac{R_1}{R_0} \tag{11}$$

Once again, comparing both regulator transfer functions given by (7) and (11) and the component relations given in (10), it can be seen that needed regulator is achieved.

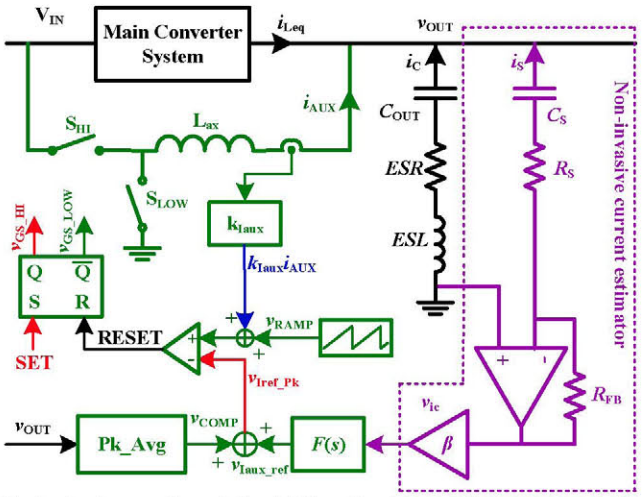

Fig. 8. Implementation of the OICC – Synchronous Buck converter with PCMC, auxiliary reference generator and current ripple compensation (green), non-invasive current estimator (purple) and the main power stage (black).

Moreover, by configuring the AMux to position 1 and closing the switch Sw, the capacitor C_S is connected between two ideal voltage sources, V^*_{REF} and the output of the operational amplifier, v_{Iref}, achieving that its dynamic does not influence the system and that its voltage is equal to the voltage of the feedback resistor R_1. Doing so, upon reconnecting the R_SC_S branch in to the feedback of the amplifier (going back to *Idle* state), the capacitor C_S is charged to correct voltage and the current of the R_SC_S branch is equal to zero. If this would not be the case, the R_SC_S branch current would affect R_1 current as step function since the current trough R_0 is constant and defined by the difference between the reference V^*_{REF} and the output voltage v_{OUT}. The step deviation of R_1 current would create a step of the main convertor inductor current reference and the system would enter in to a settling transient.

IV. Synchronous PCMC Buck OICC Implementation

The OICC implementation is presented in Fig. 8. The OICC subsystem is composed of non-invasive current estimator (purple) implemented as a simple transimpedance amplifier and designed by applying the impedance matching procedure presented in [23], the auxiliary current reference generator, the Peak to Average (Pk_Avg) offset compensation block and a High-switching frequency Synchronous buck converter with PCMC that operates as a controlled current source (CCS), shown in Fig. 1. The capacitor current estimator can be adjusted with the amplifier β and in the following analysis it is assumed that the total gain of the estimator k_{iC} is 1 V/A. When the OICC is active, the CCS is injecting an auxiliary current, i_{AUX}, at the output node composed of the mean value given by the auxiliary current reference generator v_{Iaux_ref} and the ripple component generated by the auxiliary buck converter. Since the buck converter is PCMC controlled, assuming unity gain of the inductor current sensor, k_{Iaux}, an offset between the peak current reference v_{Iref_Pk} and the mean value of the auxiliary current i_{AUX} exists due to 1) the current ripple, 2) the compensation ramp and 3) the turn on/off delays of the PCMC modulator. Therefore, the Peak to Average (Pk_Avg) offset compensation block ([21], [23]) is employed to compensate the difference by adding v_{COMP} to the auxiliary current reference voltage v_{Iaux_ref}, thus ensuring that the mean value of the auxiliary current i_{AUX} equals to the auxiliary current reference voltage v_{Iaux_ref}.

TABLE I. The Converter Specification

		Low_C_{OUT} Pr.	High_C_{OUT} Pr.
Main Conv. (2 Phase PCMC)	V_{IN}	5 V	5 V
	V_{OUT}	1.5 V	1.5 V
	R_{LL}	10 mΩ	10 mΩ
	f_{SW} per Phase	150 kHz	150 kHz
	BW_{main}	20 kHz (*Idle* st.) 8 kHz (*Active* st.)	8 kHz
	L per Phase	2 µH	2 µH
	C_{OUT}	**Ceramic: 3 x 47 µF** (ESL = ~4 nH, ESR = ~7 mΩ);	**OSCON: 2x 560 µF** (ESL = ~9 nH, ESR = ~18 mΩ); **Ceramic: 8x 100 µF** (ESL = ~2 nH, ESR = ~5 mΩ); **Ceramic: 2x 47 µF** (ESL = ~1 nH, ESR = ~5 mΩ);
	MOSFETs	SI4866BDY	SI4866BDY
	Driver	ISL6605	ISL6605
Auxiliary Conv.	f_{SW_OICC}	5 MHz	-
	L_{OICC}	100 nH	-
	n	15	-
	f_{OICCe}	50 kHz	-
	BW_{OICC}	700 kHz	-
	MOSFETs	FDMS7620S	-
	Driver	ISL6605	-

V. Experimental Results

In order to demonstrate and compare the dynamic behavior of proposed OICC system and a traditional design, two prototypes, Low_C_{OUT} and High_C_{OUT}, have been designed and built with the specifications given in Table I. Both prototypes are design to have load-line resistance of 10 mΩ and the same main converter power stage with a difference in the output capacitor implementation. The first prototype, Low_C_{OUT}, has the output capacitor of 140 µF and it utilizes the OICC in order to improve the dynamic behavior. The OICC has been implemented as a Synchronous Buck converter with PCMC which has multiplication factor of 15 and the OICC corner frequency f_{OICCe} at 50 kHz and the bandwidth BW_{OICC} of 700 kHz. On the other hand, High_C_{OUT} Prototype has been designed to have the same power stage as Low_C_{OUT} Prototype with the difference that, instead of using the OICC, it has 15 times bigger output capacitor (2.1 mF), which is implemented with 2 OSCON capacitor of 570 µF, 8 ceramic capacitors of 100 µF and 2 ceramic capacitors of 47µF.

The AVP operation is validated using an on-board resistive dummy-load, which produces load-steps of ±8 A (SR+ = 11 A/µs and SR- = -270 A/µs). The results of the experiments for Low_C_{OUT} Prototype are presented in Fig. 9 with the OICC and in Fig. 10 without the OICC. In Fig. 9 can be seen that when the load step (i_{OUT}, green) is detected, the OICC is activated and it starts to inject the auxiliary current (i_{AUX}, pink) to reduce the output voltage deviation (v_{OUT}, blue). The output voltage has smooth transition from 1.5 V (no load value) to 1.42 V (reduced by 80 mV= $R_{LL}\cdot\Delta I_{OUT}$). Also, in the output voltage, it can be seen high switching frequency ripple generated by the OICC. The whole transient lasts 50 µs. On the other hand, the Low_C_{OUT} Prototype behavior without the OICC is presented in Fig. 10, where it is shown that the output voltage has an undershoot of 380 mV while the transient lasts 160 µs, although the system have the similar bandwidth during both

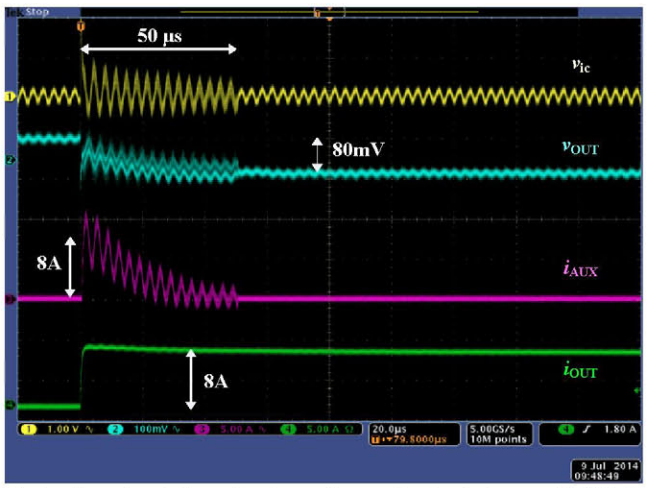

Fig. 9. Experimental results: Low_C_{OUT} – the load step-up WITH the OICC: the load current i_{OUT} (green 5A/div), the auxiliary current i_{AUX} (pink 5A/div), the output voltage v_{OUT} (blue 100mV/div), measured capacitor current v_{ic} (yellow 1 V/div) and time 20µs/div.

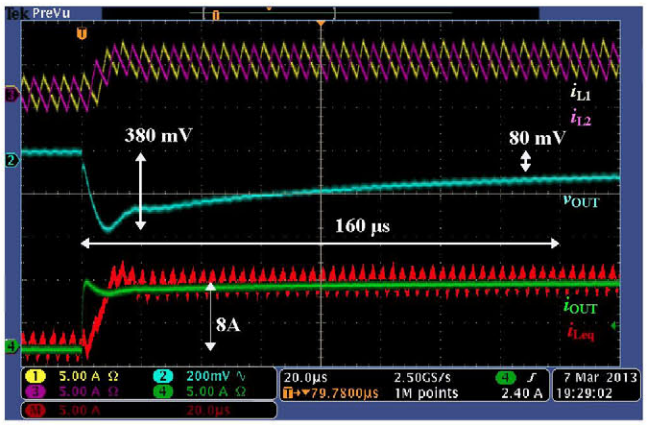

Fig. 10. Experimental results: Low_C_{OUT} – the load step-up WITHOUT the OICC: the load current i_{OUT} (green 5A/div), the first phase current i_{L1} (yellow 5A/div), the second phase current i_{L2} (pink 5A/div), sum of the first and second phase current i_{Leq} (red 5A/div) the output voltage v_{OUT} (blue 200mV/div) and time 20µs/div.

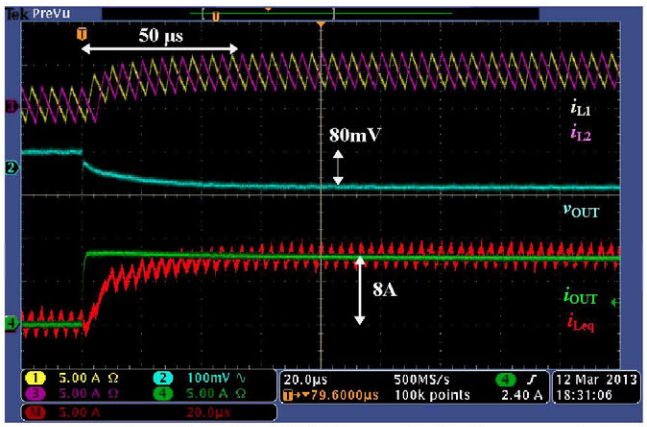

Fig. 11. Experimental results: High_C_{OUT} – the load step-up: the load current i_{OUT} (green 5A/div), the first phase current i_{L1} (yellow 5A/div), the second phase current i_{L2} (pink 5A/div), sum of the first and second phase current i_{Leq} (red 5A/div), the output voltage v_{OUT} (blue 200mV/div) and time 20µs/div.

Idle and *Active* states. The long transient is caused by the additional dynamic in the regulator, or more precise, the zero *z* of the regulator transfer function R(s) defined by (7). The regulator zero, upon closing the control loop, becomes dominant pole in the output impedance during *Idle* state and it defines the length of the transient [24]. In Fig. 10, the currents of both phases are presented (i_{L1}, yellow and i_{L2}, pink) and it can be seen that the current sharing is achieved. The results of the experiments for High_C_{OUT} Prototype are presented in Fig. 11 where it is shown that the output voltage (v_{OUT}, blue) has the same dynamic behavior as in the case of the Low_C_{OUT} Prototype with the OICC presented in Fig. 9: the voltage has a smooth transition from 1.5 V to 1.42 V, while the transient lasts 50 µs. Comparing Fig. 9 and Fig. 11, it can be concluded that the OICC concept achieves to create virtual capacitor of 2.1 mF as the one used in High_C_{OUT} Prototype.

Both prototypes have been tested for DVS operation by tracking the output voltage reference step from 1.1 V to 1.5 V and the results are presented in Fig. 12 for Low_C_{OUT} Prototype without the OICC and Fig. 13 for High _C_{OUT} Prototype. In the case of Low_C_{OUT} Prototype, the OICC is intentionally not activated since the perturbation comes from the controller and the converter operates with small output capacitor (150 µF) needing small amount of charge to change the output voltage. In Fig. 12 it can be seen that the peak of the inductor currents is increased by only 2 A. In the case of High_C_{OUT} Prototype, the output capacitor is 2.1 mF, thus the peak of the inductor currents is increased by 24 A for the same reference step. This imposes additional stress to the switches and the inductors: the design criteria needs to consider the peak of the current defined by the full load current (10 A per phase) plus the increase of the peak value to perform maximal reference step (24 A per phase for High_C_{OUT} Prototype or 2 A for Low_C_{OUT} Prototype). Furthermore, additional losses are generated due to the increased RSM currents.

In order to quantify the impact of the output capacitor on the efficiency during the DVS operation, two prototypes have been compared in terms of static and dynamic power losses. Fig. 14 presents generated power losses in steady-state operation of the two prototypes. Fig. 14*a*) shows power losses dependence on the output voltage variation under no load conditions (Low_C_{OUT}: blue, circles; High_C_{OUT}: red, squares) and with 10A output current (Low_C_{OUT}: green, diamonds; High_C_{OUT}: pink, triangles), while Fig. 14*b*) shows losses dependence on the output current with 1.5 V output voltage (Low_C_{OUT}: blue, circles; High_C_{OUT}: red, squares). As it can be seen, both prototypes have the same behavior under light load conditions, generating 537 mW of power losses with 0A load current and 1.5 V output voltage. As the output current increases (Fig. 14*b*), the power losses dependency curves starts to separate due to the slight difference of the power path resistance. At the load current of 10A Low_C_{OUT} Prototype generates 2.843W of losses, while High_C_{OUT} Prototype generates 2.738W of losses, having the losses difference of 105 mW, which is a difference of 0.7% of the converter efficiency. On the other hand, varying the output voltage in the range from 1.1V to 1.5V, the power losses have small increment since the load current is the same in all considered cases: for Low_C_{OUT} Prototype the increment of the losses at 0A load current is

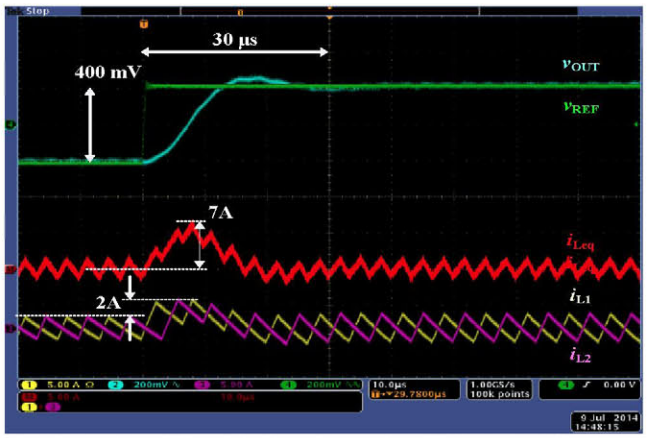

Fig. 12. Experimental results: Low_C_{OUT} – DVS: WITHOUT the OICC: the output voltage reference v_{REF} (green 200mV/div), the first phase current i_{L1} (yellow 5A/div), the second phase current i_{L2} (pink 5A/div), sum of the first and second phase current i_{Leq} (red 5A/div), the output voltage v_{OUT} (blue 200mV/div) and time 10µs/div.

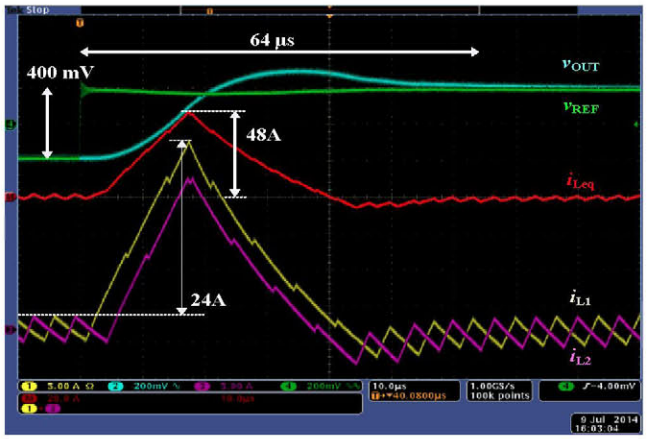

Fig. 13. Experimental results: High_C_{OUT} – DVS: the load current i_{OUT} (green 5A/div), the first phase current i_{L1} (yellow 5A/div), the second phase current i_{L2} (pink 5A/div), sum of the first and second phase current i_{Leq} (red 5A/div), the output voltage v_{OUT} (blue 200mV/div) and time 10µs/div.

88mW and 144mW at 10A load current, while for High_C_{OUT} Prototype the increment of the losses at 0A load current is 83mW and 103mW at 10A load current.

Further, the dynamic characteristics as a function of the frequency of the output voltage reference steps have been measured and presented in Fig. 15. The experiments have been performed periodically creating the output voltage reference steps from 1.1V to 1.5V and back to 1.1V with the duty cycle of 50%, while the frequency of the reference has been swept from 100 Hz up to 25 kHz. The upper limit is imposed by the bandwidth of the main converter. Fig. 15*a*) shows generated average losses of the converter, calculated as the difference of average total input power and average output power. It can be seen that, at low frequency, both systems are generating similar losses under the same conditions: 493 mW with 0A output current and 2.688 W with 10 A output current. These values of the losses corresponds to the average value of the static losses with 1.1V and 1.5V output voltages, presented in Fig. 14*a*), since the transient is negligible compared to the period. As the

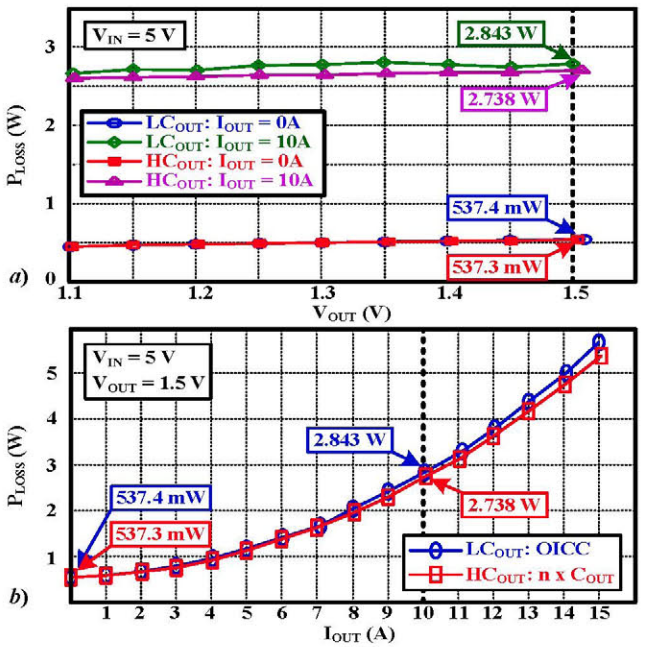

Fig. 14. Static comparison – *a*) Power Losses dependence on the output voltage: Low_C_{OUT} Prototype with I_{OUT} = 0A (blue; circles), Low_C_{OUT} Prototype with I_{OUT} =10A (green; diamonds), High_C_{OUT} Prototype with I_{OUT} = 0A (red; squares), High_C_{OUT} Prototype with I_{OUT} =10A (pink; triangles); *b*) Power Losses dependence on the output current with V_{OUT} = 1.5V: Low_C_{OUT} Prototype (blue; circles), High_C_{OUT} Prototype (red; squares).

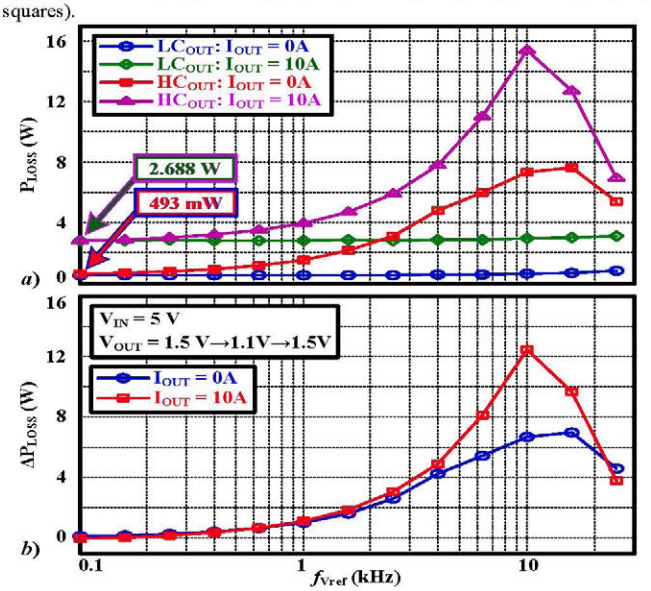

Fig. 15. Dynamic comparison – *a*) Power Losses dependence: Low_C_{OUT} Prototype with I_{OUT} = 0A (blue; circles); Low_C_{OUT} Prototype with I_{OUT} = 10A (green; diamonds); High_C_{OUT} Prototype with I_{OUT} = 0A (red; squares); High_C_{OUT} Prototype with I_{OUT} = 10A (pink; triangles): *b*) Difference of the power losses comparison.

frequency increases, the transient becomes comparable to the period of the reference steps, resulting that the losses for High_C_{OUT} Prototype have peak of 7.65W and 15.4W for 0A and 10A output current, respectively, while in the case of Low_C_{OUT} Prototype the peaks are 320 mW for both cases. These big differences in the losses are caused by higher RMS currents of the High_C_{OUT} Prototype. Fig. 15*b*) presents the

difference of the losses of both prototypes under the same conditions, showing that the peak of added losses are 6.92W for 0A output current and 12.45 W for 10 A output current.

VI. Conclusions

In this study the Output Impedance Correction Circuit (OICC) concept is extended to AVP Multiphase Current Controlled Buck converter with PCMC and compared with a system which has n times bigger output capacitor. Two 2-phase Buck converter systems with PCMC have been designed, one with the OICC system, which has multiplication factor 15 and another with 15 times bigger capacitor. Both systems exhibit the same dynamic behavior under the resistive load steps of 8 A, thus implying that the reduction of the output capacitor by factor 15 can be applied (from 2.1 mF to 140 μF). The output capacitor increase is achieved by injecting auxiliary current at the output node which is proportional to the estimated capacitor current, obtained by using a simple and easily feasible transimpedance amplifier.

Furthermore, both prototypes have been tested for DVS operation, demonstrating that the OICC approach facilitates the implementation since the switches and the inductors operate with smaller RMS currents. This is achieved by not activating the OICC subsystem during the DVS transient, thus operating with smaller output capacitor. As demonstrated in experiments, an increase of the peak value of the inductor current is 2 A per phase for the OICC design, while for the converter with 2.1 mF, the increase of the peak value is 24 A per phase. Due to the lower RMS currents generated during DVS operation, the OICC concept also improves the efficiency of the system. It has been demonstrated that the increment of the losses, due to the big capacitor employment, goes as high as 6.92W for 0A output current and 12.45 W for 10 A output current.

References

[1] INTEL Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.1 Design Guidelines (2009) [Online]. Available: www.intel.com

[2] INTEL VR12/IMVP7 sVID Protocol Rev. 1.5 (2010) [Online]. Available: www.intel.com

[3] K. Zhang, S. Luo, T. X. Wu and I. Batarseh, "New Insights on Dynamic Voltage Scaling of Multiphase Synchronous Buck Converter: A Comprehensive Design Consideration," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1927–1940, April 2014

[4] R. Redl, B. P. Erisman and Z. Zansky, "Optimizing the Load Transient Response of the Buck Converter," *in Proc. IEEE App. Power Electron. Conf. Expo.(APEC),* 1998, pp. 170–176.

[5] M. Lee, D. Chen, C. W. Liu, K. Huang, E. Tseng and B. Tai, "Comparisons of Three Control Schemes for Adaptive Voltage Position (AVP) Droop for VRMs Applications," in *Proc. IEEE Power Electronics and Motion Control Conference (EPE-PEMC)*, 2006, pp. 206–211.

[6] J. R. Huang, S.C.-H. Wang, C. J. Lee, E.K.-L. Tseng and D. Chen, "Native AVP Control Method for Constant Output Impedance of DC Power Converters," in *Proc. IEEE Power Electronics Specialists Conference (PESC)*, 2007, pp. 2023–2028.

[7] P.-H. Liu, F.C. Lee and Q. Li, "Modeling and autotuning of AVP control with inductor DCR current sensing," in *Proc. IEEE App. Power Electron. Conf. Expo.(APEC)*, 2014, pp. 1066–1072.

[8] W. Yuan, G.X. Zhang, X.G. Xie, J.M. Zhang and Z.M. Qian, "Linear-Non-Linear AVP Control with Larger Inductance for VRM," in Proc. *IEEE App. Power Electron. Conf. Expo.(APEC),* 2009, pp. 77–82.

[9] P. S. Shenoy, P. T. Krein and S. Kapat, "Beyond Time-Optimality: Energy-Based Control of Augmented Buck Converters for Near Ideal Load Transient Response," *in Proc. IEEE App. Power Electron. Conf. Expo.(APEC)*, 2011, pp. 916–922

[10] L. Amoroso, M. Donati, X. Zhou and F. C. Lee, "Single shot transient suppressor (SSTS) for high current high slew rate microprocessor," in *Proc. IEEE App. Power Electron. Conf. Expo.(APEC)*, 1999, pp. 284–288.

[11] A. Barrado, R. Vázquez, Emilio, A. Lázaro and J. Pleite, "Theoretical Study and Implementation of a Fast Transient Response Hybrid Power Supply", in *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 1003–1009, July 2004

[12] Y. Wang and D. Ma, "Ultra-Fast On-Chip Load-Current Adaptive Linear Regulator for Switch Mode Power Supply Load Transient Enhancement," in *Proc. IEEE App. Power Electron. Conf. Expo.(APEC)*, 2013, pp. 1366–1369

[13] A. M. Wu and S. R. Sanders, "An Active Clamp Circuit for Voltage Regulation Module (VRM) Applications," in *IEEE Trans. Power Electron.*, vol. 16, no. 5, pp. 623–634, Sep. 2001

[14] O. Abdel-Rahman and I. Batarseh, "Transient Response Improvement in DC-DC Converters Using Output Capacitor Current for Faster Transient Detection," in *Proc. IEEE Power Electron. Spec. Conf. (PESC),* 2007, pp. 157–160

[15] Z. Shan,S.C. Tan and C. K. Tse, "Transient Mitigation of DC–DC Converters for High Output Current Slew Rate Applications," in *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2377–2388, May 2013

[16] E. Meyer, Z. Zhang and Y.-F. Liu, "Controlled Auxiliary Circuit to Improve the Unloading Transient Response of Buck Converters,"in *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 806–819, April 2010.

[17] A. Barrado, A. Lázaro, R. Vázquez, V. Salas and E. Olías, "The Fast Response Double Buck DC–DC Converter (FRDB): Operation and Output Filter Influence," in *IEEE Trans. Power Electron.*, vol. 20 no. 6, pp. 1261–1270, Nov. 2005

[18] Y. Wen and O. Trescases, "DC-DC Converter With Digital Adaptive Slope Control in Auxiliary Phase for Optimal Transient Response and Improved Efficiency," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1314–1326, March 2012

[19] V. Šviković, J. A. Oliver, P. Alou, O. García and J. A. Cobos, "Synchronous Buck Converter with Output Impedance Correction Circuit," in *Proc. IEEE App. Power Electron. Conf. Expo.(APEC),* 2012, pp. 727–734

[20] V. Šviković, J. A. Oliver, P. Alou; O. García and J. A. Cobos, "Synchronous Buck Converter with Output Impedance Correction Circuit," in *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3415–3427, July 2013.

[21] V. Šviković, J. A. Oliver, P. Alou; O. García and J. A. Cobos, "Multiphase Current Controlled Buck Converter with Energy Recycling Output Impedance Correction Circuit (OICC)," in *Proc. IEEE App. Power Electron. Conf. Expo.(APEC)*, 2013, pp. 263–269

[22] V. Šviković, J. A. Oliver, P. Alou; O. García and J. A. Cobos, "Multiphase Current Controlled Buck Converter with Energy Recycling Output Impedance Correction Circuit (OICC)," in *IEEE Trans. Power Electron.*, vol.PP, no.99, pp.1

[23] S. C. Huerta, P. Alou, J.A. Oliver, O. Garcia and J.A. Cobos, A. Abou-Alfotouh, "Design methodology of a noninvasive sensor to measure the current of the output capacitor for a very fast non-linear control," in *Proc. IEEE App. Power Electron. Conf. Expo.(APEC),* 2009, pp. 806–811

[24] B. Choi, "Step load response of a current-mode-controlled DC-to-DC converter," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 33, no. 4, pp. 1115–1121, Oct. 1997.